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Here's the basic flow: system requirements -> fpga requirements -> plan design (block diagrams, etc.) -> write code -> simulate -> target fpga & pin planning -> synthesis & implementation -> program & test in hw -> integrate into system. I know the real answers to these questions will come from my department, but I'll take any input I can get.

r/FPGA - Guide for the implementation of Neural Network ...

The Map process maps the logic defined by an NGD file into FPGA elements, such as CLBs and IOBs. The output design is a Native Circuit Description (NCD) file that physically represents the design mapped to the components in the Xilinx FPGA. See the following table for details. For more

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information, see Running the Map Process.

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FPGA stands for "Field Programmable Gate Array". As you may already know, FPGA essentially is a huge array of gates that can be programmed and reconfigured any time anywhere. "Huge array of

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gates” is an oversimplified description of FPGA.

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